IN THE CLAIMS

Please **CANCEL** claims 1-36.

Please **ADD** new claims 37-72 as follows:

37. A process of forming an encapsulated circuit board arrangement having at least one layer of tracks, the encapsulated circuit board arrangement having a first side as an interface side and a second side as a protective cover, the process comprising the steps of:

applying at least one layer of sequentially processed tracks on a first side of an interface carrier, a second side of the interface carrier being an interface side of the encapsulated circuit board arrangement; and

joining a last applied sequentially processed layer to a support carrier with an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement.

38. The process according to claim 37, wherein the process further comprises the step of:

applying the adhesive layer on top of the last applied sequentially processed layer.

39. The process according to claim 37, wherein the process further comprises the step of:

applying the adhesive layer to the support carrier.

40. The process according to claim 37, wherein at least one of the at least one sequentially processed layer is applied using offset printing technology.

41. The process according to claim 40, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying an

acrylate as a dielectric of at least one of the at least one sequentially processed layer.

42. The process according to claim 38, wherein the adhesive layer is applied using offset printing technology.

43. The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is at least a part of a cover housing in which the encapsulated circuit board arrangement is mounted.

44. The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is at least a part of an enclosure on which the encapsulated circuit board arrangement is mounted.

45. The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is rigid.

46. The process according to claim 37, wherein the step of joining the last applied sequentially processed layer to a support carrier comprises the step of joining the last applied sequentially processed layer to a support carrier which is bendable.

47. The process according to claim 37, wherein the step of applying at

least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having connection circuitry.

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48. The process according to claim 37, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having tracks arranged as at least one passive component.

49. The process according to claim 37, wherein the step of applying at least one layer of sequentially processed tracks comprises the step of applying at least one sequentially processed layer having tracks arranged as at least one active component.

50. The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer having at least one via.

51. The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer having at least one solid via.

52. The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer that is bendable.

53. The process according to claim 37, wherein the at least one layer of sequentially processed tracks is applied to an interface layer that is made of polymide.

54. A wireless communication device, comprising:

an encapsulated circuit board arrangement manufactured by applying at least

one layer of sequentially processed tracks on a first side of an interface carrier, a second side of the interface carrier being an interface side of the encapsulated circuit board arrangement; and

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joining a last applied sequentially processed layer to a support carrier with an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement.

55. A wireless mobile terminal, comprising:

an encapsulated circuit board arrangement manufactured by applying at least one layer of sequentially processed tracks on a first side of an interface carrier, a second side of the interface carrier being an interface side of the encapsulated circuit board arrangement; and

joining a last applied sequentially processed layer to a support carrier with an adhesive layer, the support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement.

56. An encapsulated circuit board arrangement having at least one sequentially processed track layer, the encapsulated circuit board arrangement having a first side as an interface side and a second side as a protective cover, wherein the circuit board arrangement comprises:

an interface carrier having a first side and a second side, a first side of the interface carrier being the interface side of the encapsulated circuit,

at least one layer of sequentially processed tracks on the second side of the interface carrier;

a support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement; and

an adhesive layer arranged between a top surface of a last sequentially processed layer and the support carrier.

57. The circuit board arrangement according to claim 56, wherein at least one of the at least one sequentially processed layer is applied using offset printing technology.

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58. The circuit board arrangement according to claim 56, wherein a dielectric of at least one of the at least one sequentially processed layer is acrylate.

59. The circuit board arrangement according to claim 56, wherein the adhesive layer is applied using offset printing technology.

60. The circuit board arrangement according to claim 56, wherein the support carrier is at least a part of a cover housing in which the encapsulated circuit is mounted.

61. The circuit board arrangement according to claim 56, wherein the support carrier is at least a part of an enclosure on which the encapsulated circuit board arrangement is mounted.

62. The circuit board arrangement according to claim 56, wherein the support carrier is rigid.

63. The circuit board arrangement according to claim 56, wherein the support carrier is bendable.

64. The circuit board arrangement according to claim 56, wherein at least one of the at least one sequentially processed layer includes connection circuitry.

65. The circuit board arrangement according to claim 56, wherein at least one of the at least one sequentially processed layer includes tracks arranged as at

least one passive component.

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66. The circuit board arrangement according to claim 56, wherein at least one of the at least one sequentially processed layer includes tracks arranged as at least one active component.

67. The circuit board arrangement according to claim 56, wherein the interface layer includes at least one via.

68. The circuit board arrangement according to claim 67, wherein at least one of the at least one via is solid.

69. The circuit board arrangement according to claim 56, wherein the interface carrier is bondable.

70. The circuit board arrangement according to claim 56, wherein the interface carrier includes polymide.

71. A wireless communication device, comprising:

an encapsulated circuit board arrangement having an interface carrier having a first side and a second side, a first side of the interface carrier being the interface side of the encapsulated circuit,

at least one layer of sequentially processed tracks on the second side of the interface carrier;

a support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement; and

an adhesive layer arranged between a top surface of a last sequentially processed layer and the support carrier.

72. A wireless mobile terminal, comprising:

an encapsulated circuit board arrangement having an interface carrier having a first side and a second side, a first side of the interface carrier being the interface side of the encapsulated circuit,

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at least one layer of sequentially processed tracks on the second side of the interface carrier;

a support carrier forming the protective cover of the second side of the encapsulated circuit board arrangement; and

an adhesive layer arranged between a top surface of a last sequentially processed layer and the support carrier.